46. (new) A method of fabricating a field-effect device on an integrated circuit, comprising the steps of:

providing a single-crystal silicon substrate;

forming a zirconium silicate dielectric layer on the substrate; and

forming a conductive gate overlying the zirconium silicate dielectric layer.

47. (new) The method of claim 46, wherein the forming a zirconium silicate dielectric layer step comprises:

exposing a clean Si surface on the substrate;

depositing zirconium on the Si surface;

annealing the substrate in an inert ambient, thereby forming a layer of zirconium silicide on the substrate;

oxidizing the layer of zirconium silicide, thereby forming the zirconium silicate dielectric layer.

48. (new) The method of claim 47, further comprising oxidizing less than 1 nanometer of the clean Si surface prior to the depositing zirconium step.

49. (new) The method of claim 47, wherein the oxidizing step comprises simultaneous exposure of the layer of zirconium silicide to an oxidizing gas and a reducing gas.

50. (new) The method of claim 49, wherein the oxidizing gas is selected from the group consisting of O_2, H_2O, N_2O, CO_2, and combinations thereof.

51. (new) The method of claim 49, wherein the reducing gas is selected from the group consisting of CO, H_2, CH_3, and combinations thereof.

52. (new) The method of claim 49, wherein the oxidizing gas is selected from the group consisting of O_2, H_2O, N_2O, CO_2, and combinations thereof , and wherein the reducing gas is selected from the group consisting of CO, H_2, CH_3, and combinations thereof.

53. (new) The method of claim 47, wherein the oxidizing step comprises exposure of the layer of a silicide to an oxygen plasma.

54. (new) The method of claim 53, wherein the oxygen plasma is exposed to ultraviolet radiation.

55. (new) The method of claim 47, further comprising annealing the zirconium silicate layer in a non-oxidizing environment, thereby densifying the silicate layer.

56. (new) The method of claim 55, wherein the annealing step is carried out at a temperature sufficient to crystallize the silicate layer.

57. (new) The method of claim 46, wherein the forming a zirconium silicate dielectric layer step comprises:

depositing zirconium on the substrate in an oxidizing ambient, thereby forming an at least partially oxidized layer on the substrate; and

annealing the substrate in an oxidizing ambient.

58. (new) The method of claim 57, wherein the substrate comprises an oxidized silicon surface layer immediately prior to the depositing step.

59. (new) The method of claim 57, wherein the substrate comprises a clean Si surface immediately prior to the depositing step.

60. (new) The method of claim 57, wherein the depositing zirconium step comprises sputtering material from a target of zirconium onto the substrate.

61. (new) The method of claim 46, wherein the forming a zirconium silicate dielectric layer step comprises:

depositing zirconium and silicon on the substrate in an oxidizing ambient, thereby forming an at least partially oxidized layer on the substrate; and

annealing the substrate in an oxidizing ambient.

62. (new) The method of claim 61, wherein the substrate comprises an oxidized silicon surface layer immediately prior to the depositing step.

63. (new) The method of claim 61, wherein the substrate comprises a clean Si surface immediately prior to the depositing step.

64. (new) The method of claim 61, wherein the depositing zirconium and silicon step comprises simultaneous deposition of a layer comprising zirconium and silicon.

65. (new) The method of claim 64, wherein the simultaneous deposition comprises sputtering material from a target comprised of the zirconium and silicon onto the substrate.

66. (new) The method of claim 64, wherein the simultaneous deposition comprises evaporating zirconium and silicon from a common source.

67. (new) The method of claim 64, wherein the simultaneous deposition comprises evaporating zirconium and silicon from separate sources.

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68. (new) The method of claim 67, wherein the evaporation rate of the separate sources are independently varied during the depositing step, thereby forming a zirconium silicate dielectric layer having a depth-varying ratio of zirconium to silicon.

69. 24 (new) The method of claim 46, wherein the forming a zirconium silicate dielectric layer step comprises the repeated steps of:

evaporating an intermediate layer of material onto the substrate, the material selected from the group consisting of silicon, zirconium, and combinations thereof, the intermediate layer having a thickness less than 1 nanometer; and

D4 annealing the substrate in an oxidizing ambient, thereby at least partially oxidizing the intermediate layer.

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70. (new) The method of claim 69, wherein a first set of one or more of the intermediate layers are silicon, and a second set of one or more of the intermediate layers comprise zirconium, the first set of layers and the second set of layers being deposited in alternating fashion.

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71. (new) The method of claim 46, wherein the forming a zirconium silicate dielectric layer step comprises:

exposing a clean Si surface on the substrate; and

depositing a partially reduced zirconium silicate layer on the Si surface.

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72. (new) The method of claim 71, further comprising annealing the partially reduced zirconium silicate layer substrate in oxygen, thereby forming the zirconium silicate dielectric layer.

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73. (new) The method of claim 72, wherein the depositing a partially reduced zirconium silicate layer on the Si surface comprises simultaneous physical vapor deposition of zirconium oxide and silicon.

74-80

74. (new) An integrated circuit made by the method of claim 1.

75. (new) An integrated circuit made by the method of claim 46.

76. (new) An integrated circuit made by the method of claim 47.

77. (new) An integrated circuit made by the method of claim 57.

DY

78. (new) An integrated circuit made by the method of claim 61.

79. (new) An integrated circuit made by the method of claim 69 .

80. (new) An integrated circuit made by the method of claim 71.